OKI semiconductor

MSM6962/6982(μ-Law)
MSM6963/6983(A-Law)

SINGLE CHIP CODEC WITH FILTER

GENERAL DESCRIPTION

MSM6962, MSM6982, MSM6963 and MSM6983 are CMOS devices that contain a companding CODEC and PCM filters on a single chip. It converts voice signals to PCM signals (μ-law or A-law) and vice versa. It contains analog pre-filter, transmit switched capacitor filter (SCF), receive SCF, analog post-filter and CODEC.

The transmit section and the receive section are designed to operate in both synchronous and asychronous applications.

Each section requires sampling clock (8 kHz) and data clock (512 kHz, 1024 kHz, 1536 kHz, 1544 kHz or 2048 kHz) respectively.

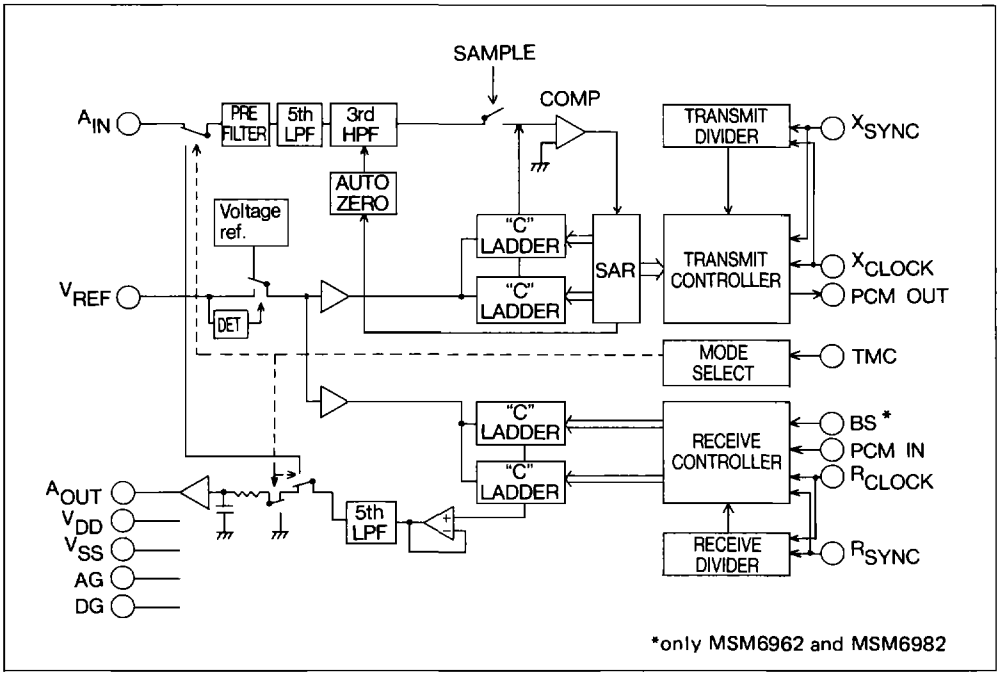
FEATURES

- Per-channel Single Chip CODEC with Filters.
- ±5 V Power Supplies
- Low Power Dissipation
  55 mW operating (TYP)
  4 mW standby (TYP)
- Follows the μ-companding Law. (MSM-6962 and MSM6982)
- Follows the A-companding Law. (MSM-6963 and MSM6983)
- Synchronous or Asynchronous Operation.
- Serial Data Rate of 512KBPS, 1024-KBPS, 1536KBPS, 1544KBPS or 2048-KBPS.
- On-chip Full Auto-ZERO Circuit.
- On-chip Analog Pre-Filter and Post-Filter.
- Excellent Power Supply Rejection Ratio
  30 dB (from 300 Hz to 300 kHz)
- On-chip Precision Voltage reference.

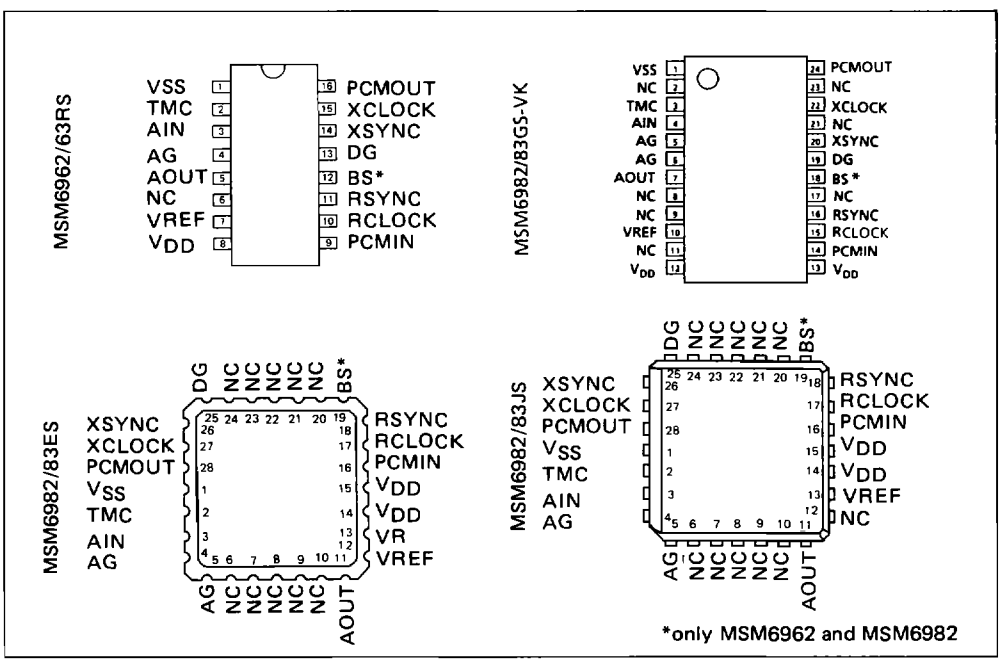
PACKAGE VARIETY

μ-Law	A-Law	Package	No. of Pin
MSM6962RS	MSM6963RS	Plastic DIP	16 (DIP16-P-300)
MSM6982JS	MSM6983JS	Plastic QFJ (PLCC)	28 (QFJ28-P-S450)
MSM6982ES	MSM6983ES	Ceramic QFN (LCC)	28 (QFN28-G-S450, C-S450)
MSM6982GS-VK	MSM6983GS-VK	Plastic SOP	24 (SOP24-P-430-VK)

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ +7	V
	V_{SS}	+0.3 ~ -7	V
Reference Voltage	V_{REF}	0 ~ V_{DD}	V
Analog Input Voltage	V_{AIN}	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	-0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_{OP}	-10 ~ 80	°C
Storage Temperature	T_{stg}	-55 ~ 150	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.75	5	5.25	V
	V_{SS}		-5.25	-5	-4.75	V
Reference Voltage	V_{REF}		—	2.5	—	V
Analog Input Voltage	V_{AIN}		—	—	5	Vpp
Input High Voltage	V_{IH}	XSYNC, XCLOCK, PCM IN, RSYNC, RCLOCK, TMC, BS	2.0	—	V_{DD}	V
Input Low Voltage	V_{IL}		0	—	0.8	V
Clock Frequency	f_c	XCLOCK, RCLOCK	512, 1024 1536, 1544, 2048			kHz
Sync Pulse Frequency	f_s	XCLOCK, RSYNC	—	8	—	kHz
Clock Duty Ratio	D_R	XCLOCK, RCLOCK	40	50	60	%
Digital Input Rise Time	t_{Ir}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	—	—	50	ns
Digital Input Fall Time	t_{Ir}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	—	—	50	ns
XMIT. Sync Timing	t_{XS}	XCLOCK → XSYNC (Fig. 3)	50	—	—	ns
	t_{SX}	XSYNC → XCLOCK (Fig. 3)	150	—	—	ns
RCV. Sync Timing	t_{RS}	RCLOCK → RSYNC (Fig. 3)	50	—	—	ns
	t_{SR}	RSYNC → RCLOCK (Fig. 3)	100	—	—	ns
XMIT. Sync Pulse Width	t_{WX}	(Fig. 3)	1/fc	—	117	μs
RCV. Sync Pulse Width	t_{WR}	(Fig. 3)	1/fc	—	117	μs
PCM IN Set-up Time	t_{DS}	(Fig. 3)	100	—	—	ns
PCM IN Hold Time	t_{DH}	(Fig. 3)	100	—	—	ns
Analog Output Allowable Load	R_{AL}		10	—	—	kΩ
	C_{AL}		—	—	100	PF
Digital Output Allowable Load	R_{DL}		1	—	—	kΩ
	C_{DL}		—	—	100	PF
Operating Temperature	T_{OP}		0	—	70	°C

DC Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Supply Current (Operating)	I_{DD1}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		–	5.5	11	mA
	I_{SS1}			–	5.0	11	mA
Supply Current (Stand-by)	I_{DD2}			–	1.0	3	mA
	I_{SS2}			–	0.3	1.5	mA
Reference Current	I_{REF}			–	5	100	μA
Input High Voltage	V_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		2.0	1.7	–	V
Input Low Voltage	V_{IL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		–	1.6	0.8	V
Input Leakage Current	I_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V	V_I = 5 V	–	< 0.5	2.0	μA
	I_{IL}		V_I = 0 V	–	< 0.5	0.5	μA
Output Low Voltage	V_{OL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		–	< 0.2	0.4	V
Output Leakage Current	I_{OH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		–	< 5	10	μA
Input Capacitance	C_{IN}	Except for AIN		–	5	–	PF
		AIN		–	5	–	PF
Analog Input Resistance	R_{IN}	f_{IN} < 3.4 kHz		–	1	–	MΩ

AC Characteristics

V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, V_R = 0 V

Parameter	Symbol	Condition f (Hz)	Condition Level (dBmO)		Min	Typ	Max	Unit
Transmit Frequency Response	Loss T1	60	0		20	26	–	dB
	Loss T2	300			−0.1	−0.03	0.2	
	Loss T3	820			Reference Value			
	Loss T4	2020			−0.1	0.0	0.2	
	Loss T5	3000			−0.1	0.10	0.2	
	Loss T6	3400			0	0.45	0.8	
	Loss T7	3980			14	16	–	
Receive Frequency Response	Loss R1	300	0		−0.1	−0.02	0.2	dB
	Loss R2	820			Reference Value			
	Loss R3	2020			−0.1	0.0	0.2	
	Loss R4	3000			−0.1	0.10	0.2	
	Loss R5	3400			0	0.65	0.8	
	Loss R6	3980			14	16	–	
Transmit Signal to Distortion Ratio (*1)	SD T1	1020	3		36	43	–	dB
	SD T2		0		36	41	–	
	SD T3		−30		36	40	–	
	SD T4		−40	*2	31	34.5 / 33	–	
	SD T5		−45	*2	26	31 / 28.5	–	
Receive Signal to Distortion Ratio (*1)	SD R1	1020	3		36	44	–	dB
	SD R2		0		36	41	–	
	SD R3		−30		36	41	–	
	SD R4		−40	*2	31	35.5 / 35	–	
	SD R5		−45	*2	26	34 / 28.5	–	

*1 : The measurement is taken with P-message filter.

*2 : MSM6962 MSM6982 / MSM6963 MSM6983

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Transmit Gain Tracking		GT T1	1020	3	-0.2	-0.01	0.2	dB
		GT T2		-10	Reference Value			
		GT T3		-40	-0.2	0.05	0.2	
		GT T4		-50	-0.4	0.25	0.4	
		GT T5		-55	-0.8	0.10	0.8	
Receive Gain Tracking		GT R1	1020	3	-0.2	0.02	0.2	
		GT R2		-10	Reference Value			
		GT R3		-40	-0.2	-0.05	0.2	
		GT R4		-50	-0.4	-0.16	0.4	
		GT R5		-55	-0.8	-0.13	0.8	
Idle Channel Noise *3	Transmit	N_{IDL} T		–	–	-89	-75	dBmOp
	Receive	N_{IDL} R	–	–	–	-89	-75	
Analog Input Level		V_{IN}	1020	0	1.182	1.252	1.326	Vrms
Analog Output Level		V_{OUT}	1020	0	1.182	1.252	1.326	Vrms
Absolute Delay Time		t_D	–	–	–	0.47	0.5	ms
Transmit Group Delay Time		t_{GD} T1	500	0	–	0.2	0.75	ms
		t_{GD} T2	600		–	0.1	0.35	
		t_{GD} T3	1000		–	0	0.125	
		t_{GD} T4	1800		Reference Value			
		t_{GD} T5	2600		–	0.05	0.125	
		t_{GD} T6	2800		–	0.07	0.75	
Receive Group Delay Time		t_{GD} R1	500	0	–	-0.02	0.75	ms
		t_{GD} R2	600		–	-0.02	0.35	
		t_{GD} R3	1000		–	0.03	0.125	
		t_{GD} R4	1800		Reference Value			
		t_{GD} R5	2600		–	0.07	0.125	
		t_{GD} R6	2800		–	0.10	0.75	

*3 : The measurement is taken with P-message filter.

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Crosstalk	T to R	C_R T	1020	0	–	-90	-66	dBmO
	R to T	C_R R	1020		–	-78	-66	
Discrimination Against Out-of-Band Input Signals		DIS	4.6K ~ 72K	-25	30	32	–	dB
Spurious Out-of-band Signals at the Output		SO	300 ~ 3400	0	–	-33	-30	dBmO
Intermodulation		IMD 1	fa=470 fb=320	-4	–	-40	-38	dB
Spurious In-band Signals at the Output		SI	1020	0	–	-45	-40	dBmO
Single Frequency Noise		N_S	–	–	–	-60	-50	dBmO
V_{DD} PSRR	Transmit	PPSR T	0 ~ 300K	200 mVp-p	–	30	–	dB
	Receive	PPSR R			–	30	–	
V_{SS} PSRR	Transmit	NPSR T			–	30	–	dB
	Receive	NPSR R			–	30	–	
Digital Output Delay Time		t_{SD}	R pull = 1 kΩ C_L = 100 pF		50	150	200	ns
		t_{XD_1}			50	100	200	
		t_{XD_2}			50	100	200	
		t_{XD_3}			50	180	200	
Digital Output Fall Time		t_{DDf}			–	20	100	ns

PIN DESCRIPTION

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>ES,JS</th><th>GS-VK</th></tr>
<tr><td>V_{SS}</td><td>1</td><td>1</td><td>1</td><td>V_{SS} is a negative supply pin. The voltage supplied to this pin should be -5 V ±5%.</td></tr>
<tr><td>TMC</td><td>2</td><td>2</td><td>3</td><td>Test mode control input pin.
TMC is a control input for operating mode selection, such as normal operating mode and analog loop-back mode.
The operating modes are listed in the following table.
<table>
<tr><th>"TMC"</th><th>Mode</th><th>"AOUT"</th><th>"AIN"</th></tr>
<tr><td>V_{IH} (2.0V ~ V_{DD})</td><td>Operating</td><td>Receive signal output Connected to to RCV_{FIL} output</td><td>Xmit signal input</td></tr>
<tr><td>V_{IL} (0 ~ 0.8V)</td><td>Analog Loop back (Refer to Fig. 1)</td><td>ov</td><td>Disconnected</td></tr>
</table></td></tr>
<tr><td>AIN</td><td>3</td><td>3</td><td>4</td><td>AIN is a analog signal input pin and is normally connected to the transmit filter input. The input analog signal is bandwidth-limited to 3.4 kHz and is converted to the 8 bits PCM signal.
The input analog signal must remain between + VREF and - VREF for accurate conversion.
In the analog loop-back mode, this pin is disconnected from any other circuits.</td></tr>
<tr><td>AG</td><td>4</td><td>4,5</td><td>5,6</td><td>Analog ground pin.
AG is connected to the analog system ground.</td></tr>
<tr><td>A_{OUT}</td><td>5</td><td>11</td><td>7</td><td>A_{OUT} is a analog signal output pin and is connected to the receive filter output.
The output voltage range is ±2.5 V.</td></tr>
<tr><td>V_{REF}</td><td>7</td><td>13</td><td>10</td><td>V_{REF} is an input pin of the external voltage reference. This pin is left in open or connected to AG to activate the internal voltage reference.</td></tr>
<tr><td>V_{DD}</td><td>8</td><td>14, 15</td><td>12,13</td><td>V_{DD} is a positive supply pin. The voltage supplied to this pin should be +5 V ±5%.</td></tr>
<tr><td>PCM_{IN}</td><td>9</td><td>16</td><td>14</td><td>PCM_{IN} is an input pin of the PCM signal. This signal is serial data and is converted to the analog signal under control of R_{SYNC} and R_{CLOCK}. The input PCM data rates are 512KBPS, 1024KBPS, 1536KBPS, 1544KBPS or 2048KBPS.</td></tr>
</table>

Pin Name	Pin No.			Function
	RS	ES, JS	GS-VK	
R_{CLOCK}	10	17	15	R_{CLOCK} is an input pin of the clock that provides the basic timing and control signals required for the input of the PCM signal. The frequency of this clock must be coincident with the input PCM data rate.
R_{SYNC}	11	18	16	R_{SYNC} is an input pin of the pulse signal that is synchronized with R_{CLOCK} and is used for taking out the required signal from the input serial PCM data. This signal makes the whole operation in the receive section synchronized. When R_{SYNC} is connected continuously low or continuously high, the receive section is powered down. The frequency of this signal is 8 kHz ±50 ppm.
BS	12	19	18	7 bit decode control input pin. In the normal mode and the analog loop back mode, a positive or negative transient of BS signal provides a 7 bits decode operation with MSM6962 and MSM6982. (Refer to Fig. 4)
DG	13	25	19	Digital ground pin. DG is connected to the digital system ground.
X_{SYNC}	14	26	20	X_{SYNC} is an input pin of the pulse signal that is synchronized with X_{CLOCK} and makes the whole operation in the transmit section synchronized. The output signal from the PCM_{OUT} pin is naturally synchronized with this signal. When X_{SYNC} is connected continuously low or continuously high, the transmit section is powered down. The frequency of this signal is 8 kHz ±50 ppm.
X_{CLOCK}	15	27	22	X_{CLOCK} is an input pin of the clock that provides the basic timing and control signals required for the output of PCM signal. Clock rates of 512KBPS, 1024KBPS, 1536KBPS, 1544KBPS or 2048KBPS can be used for X_{CLOCK}.
PCM_{OUT}	16	28	24	PCM_{OUT} is an output pin of the PCM signal. The result of conversion from analog to digital is output from this pin as 8 bits serial data. This data is shifted out under control of X_{SYNC} and X_{CLOCK}. Because of an open-drain output, wired-OR connections are easily performed.

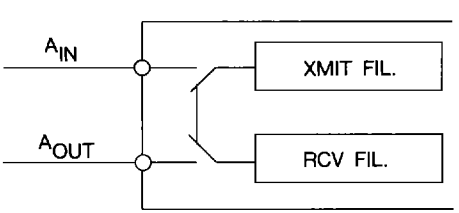
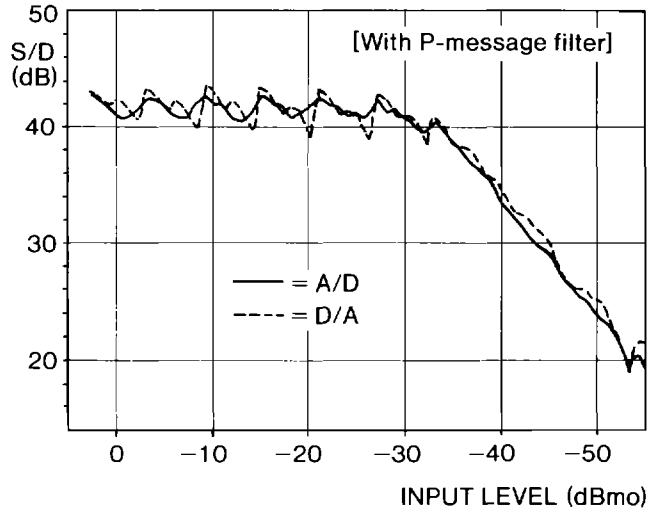
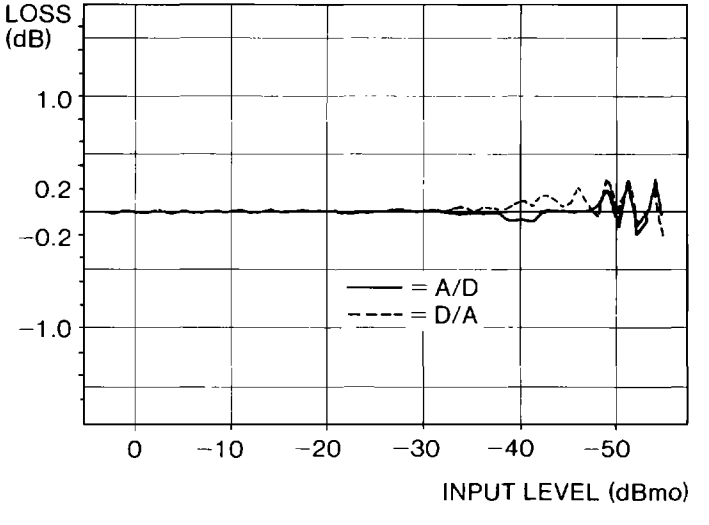


Figure 1

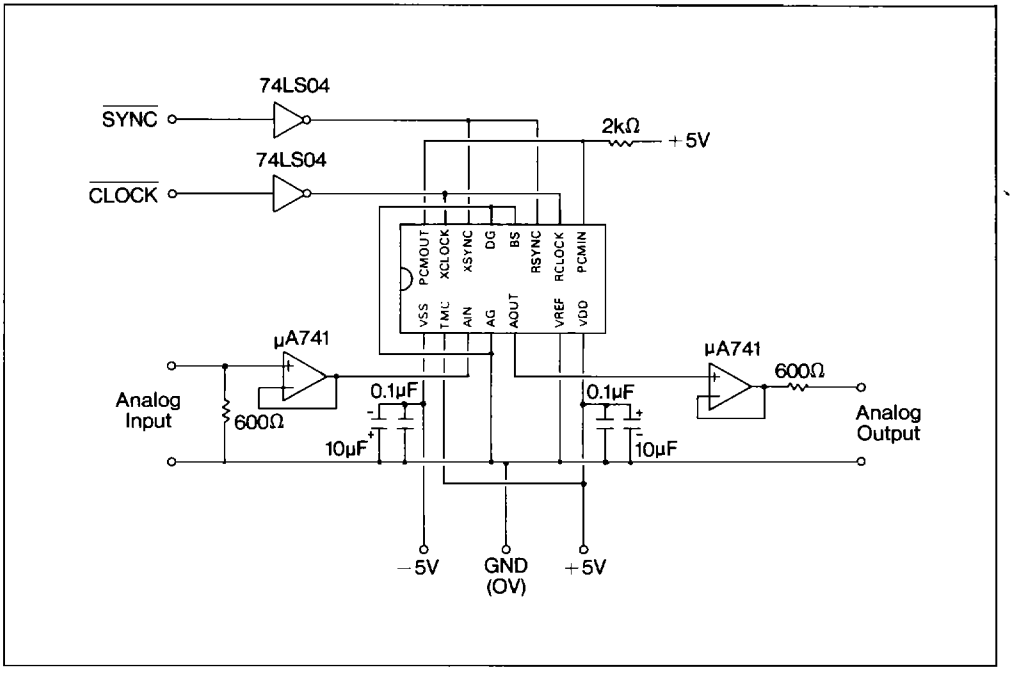
SIGNAL TO DISTORTION RATIO



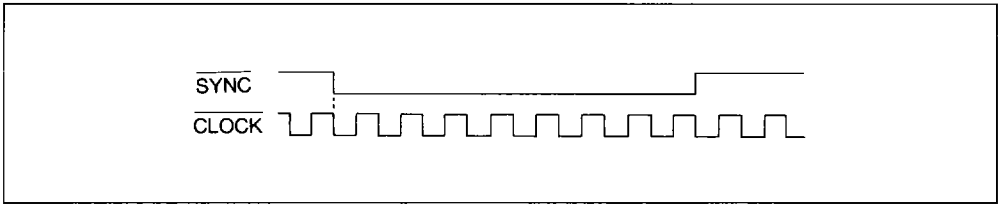
GAIN TRACKING CHARACTERISTICS



TEST CIRCUIT FOR MSM6962 AND MSM6963



Note 1: SYNC and CLOCK timing.



Note 2: Make the connection wire between AG and DG as short as possible.
Note 3: Use a test socket with short leads.

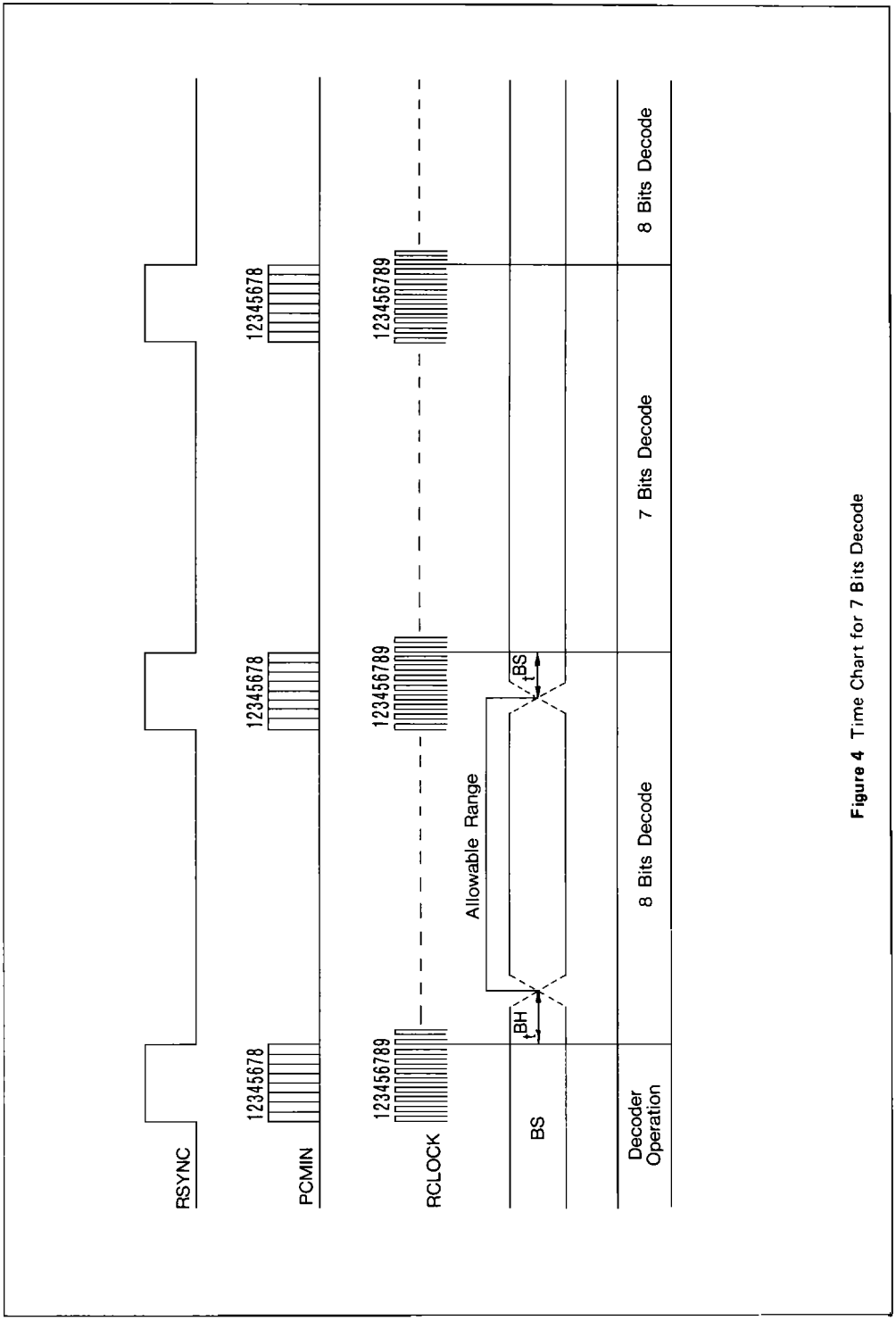


Figure 4 Time Chart for 7 Bits Decode

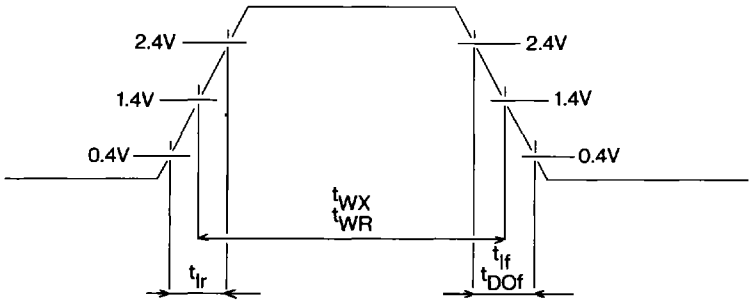


Figure 2 Definitions of Rise Time and Fall Time

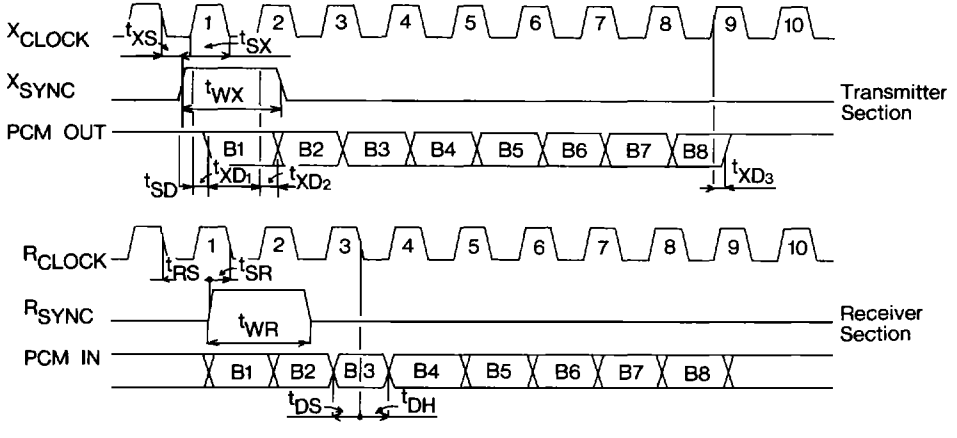


Figure 3 Basic Time Chart